WHAT IS CLAIMED IS:

1. A synchronization circuit for receiving an input signal and a clock having a frequency equal to a transfer rate of the input signal, and synchronizing the input signal with the clock, said circuit comprising:

a state detection circuit for outputting a control signal according to the temporal relationship between a transition point of the input signal and an edge of the clock;

a delay selection circuit for adding a delay to the input signal on the basis of the control signal; and

a latch circuit for synchronizing the signal outputted from the delay selection circuit with the clock, and outputting the synchronized signal.

2. A synchronization circuit for receiving an input signal and a clock having a frequency equal to a transfer rate of the input signal, and synchronizing the input signal with the clock, said circuit comprising:

a state detection circuit for outputting a control signal according to the temporal relationship between a transition point of the input signal and an edge of the clock;

a delay selection circuit for adding a delay to the clock on the basis of the control signal; and

a latch circuit for synchronizing the input signal with the clock outputted from the delay selection circuit, and outputting

the synchronized signal.

3. A synchronization circuit for receiving plural input signals having phases irrelevant to each other, and a clock having a frequency equal to a transfer rate of the plural input signals, and synchronizing the plural input signals with the clock, said circuit comprising:

a state detection circuit for outputting control signals relating to the respective input signals, according to the temporal relationship between transition points of the plural input signals;

a delay selection circuit for adding delays to the respective input signals on the basis of the control signals relating to the respective input signals; and

a latch circuit for synchronizing the respective signals outputted from the delay selection circuit with the clock, and outputting the synchronized signals.

4. A synchronization circuit for receiving plural signal bundles each comprising a set of plural input signals synchronized with each other and a single clock having a frequency equal to a transfer rate of the plural input signals, in which the phases of the input signals included in one signal bundle are irrelevant to the phases of the input signals included in the other signal bundles, and synchronizing the input signals included in one

signal bundle with the input signals included in the other signal bundles by using a single synchronization clock that is selected from among the clocks included in the respective signal bundles, said circuit comprising:

a state detection circuit for detecting the state between the plural input signals included in the respective signal bundles;

a clock selection circuit for receiving the clocks included in the respective signal bundles, and selecting one of the inputted clocks, as a synchronization clock, on the basis of the result of the state detection performed between the respective signal bundles by the state detection circuit;

a delay selection circuit for adding delays to the plural input signals included in each signal bundle, on the basis of the result of the state detection performed between the respective signal bundles; and

a latch circuit for synchronizing the output signal from the delay selection circuit for each signal bundle, with the synchronization clock, and outputting the synchronized signal.

5. A synchronization circuit as defined in Claim 4 wherein said state detection circuit comprises:

an early/late detection circuit for detecting which signal bundle is earlier in input timing between the respective signal bundles, and outputting an early/late detection signal; and

an overlap detection circuit for detecting an overlap period between the respective signal bundles, and outputting an overlap detection signal;

said clock selection circuit selects, as a synchronization clock, a clock included in a signal bundle which is determined as being inputted earlier between the respective signal bundles, on the basis of the early/late detection signal; and

said delay selection circuit adds delays based on the early/late detection signal and the overlap detection signal, to the plural input signals included in the respective signal bundles.

6. A synchronization circuit as defined in Claim 1 wherein said delay selection circuit comprises:

a delay circuit for adding a delay to the input signal; and

a selection circuit for selecting either the input signal or the output signal of the delay circuit on the basis of the control signal.

7. A synchronization circuit as defined in Claim 2 wherein said delay selection circuit comprises:

a delay circuit for adding a delay to the inputted clock; and

a selection circuit for selecting either the inputted clock or the clock outputted from the delay circuit on the basis of the control signal.

8. A synchronization circuit as defined in Claim 3, wherein said delay selection circuit comprises:

a delay circuit for adding delays to the respective input signals; and

a selection circuit for selecting one from among the plural input signals and the signals outputted from the delay circuit, for each of the plural input signals, on the basis of the control signals relating to the respective input signals, and outputting the selected signal.

9. A synchronization circuit as defined in any of Claims 1 to 5 wherein

said state detection circuit detects the state of the input signal on the basis of a preamble detection signal which is supplied from the outside and indicates the positional relationship of data to be synchronized.